

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY  
HYDERABAD

IV Year B.Tech. ECE.II-Sem

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DIGITAL DESIGN THROUGH VERILOG  
(ELECTIVE – III)

**UNIT I**

**INTRODUCTION TO VERILOG** : Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

**LANGUAGE CONSTRUCTS AND CONVENTIONS** : Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

**UNIT II**

**GATE LEVEL MODELING** : Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.

**UNIT III**

**BEHAVIORAL MODELING** : Introduction, Operations and Assignments, Functional Bifurcation, *Initial* Construct, *Always* Construct, Examples, Assignments with Delays, *Wait* construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non blocking Assignments, The *case* statement, Simulation Flow. *if* and *if-else* constructs, *assign-deassign* construct, *repeat* construct, *for* loop, the *disable* construct, *while* loop, *forever* loop, parallel blocks, *force-release* construct, Event.

**UNIT IV**

**MODELING AT DATA FLOW LEVEL** : Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators.

**SWITCH LEVEL MODELING.**

Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.

**UNIT V**

**SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES** : Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises,

**FUNCTIONS, TASKS, AND USER-DEFINED PRIMITIVES** : Introduction, Function, Tasks, User- Defined Primitives (UDP), FSM Design (Moore and Mealy Machines)

**UNIT VI**

**DIGITAL DESIGN WITH SM CHARTS** : State Machine Charts, Derivation of SM Charts, Realization of SM Charts, Implementation of the Dice Game, Alternative realizations for SM Charts using Microprogramming, Linked State Machines.

**UNIT VII**

**DESIGNING WITH PROGRAMMABLE GATE ARRAYS AND COMPLEX PROGRAMMABLE**

**LOGIC DEVICES** : Xilinx 3000 Series FPGAs, Designing with FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs.

**UNIT VIII**

**VERILOG MODELS** : Static RAM Memory, A simplified 486 Bus Model, Interfacing Memory to a Microprocessor Bus, UART Design, Design of Microcontroller CPU.

**TEST BOOKS :**

1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, 2004 IEEE Press.
2. A Verilog Primer – J. Bhaskar, BSP, 2003.

**REFERENCES :**

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.
2. Digital Systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.

3. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.
4. Digital systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.